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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Matthew J. Adiletta, et al.
Serial No. : 09/387,109
Filed : August 31, 1999
Title : SDRAM CONTROLLER FOR PARALLEL PROCESSOR ARCHITECTURE

Art Unit : 2183
Examiner : Unknown

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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APR 28 2004

INFORMATION DISCLOSURE STATEMENT Technology Center 2100

Applicant submits the references listed on the attached form PTO-1449. Applicant has not provided copies of the US patents in accordance with the waiver posted on the USPTO website.

This statement is being filed within three months of the filing date of the application or before the receipt of a first Office action on the merits. Please apply any charges or credits to deposit account 06-1050, 10559-079001.

Respectfully submitted,

Date:

4/23/04

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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

23 April 2004

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